وقائع المؤتمر العلمي السنوي الثالث لكلية التربية الاساسية
في مجال العلوم الصرفة والموسوم:
(مؤتمر كلية التربية الاساسية في مجال العلوم الصرفة)
وتحت شعار
(بالعلوم الصرفة نبني واقعا معرفيا متجددا)
يومي الاحد والاثنين 21-2026/6/22

Intelligent System for Monitor and Control the Gas Pollution via FPGA & GSM

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Abstract:
FPGAs have the ability to parallel processing and this fast processing gives real-time timing and performance requirements for industrial applications. The objective of project is to by sensor connected through the FPGA control unit, which reads the data and processes it. The interface circuit in FPGA control unit connected to the GSM modem. If pollution values exceed the permissible levels of pollution, an alert will be sent to the operator, other people concerned and SMS via GSM. The aim of the project is to design FPGA industrial application for measure the gas pollution in order to achieve greater system integration and reduce cost in development .

Keywords: FPGA ,GSM ,VHDL ,HDL ,MQ-135 ,CLBs ,IOBs ,LUTs ,JTAG.

I. Introduction:

The air we breathe is a growing concern for people worldwide. The World Health Organization reports that over 90% of the global population inhales polluted air daily [1,2]. This isn't merely an environmental issue; it's a serious public health crisis. Exposure to air pollution, whether brief or prolonged, can cause severe health problems. These include lung cancer, heart disease, strokes, and can even result in premature death [3,4,5].

The danger is not limited to the outdoors. Because modern populations spend roughly 80% to 90% of their time inside, indoor air quality often has a more direct impact on human health than the outside atmosphere [6,7,8,9]. Furthermore, in industrial settings, human error or mechanical failure can lead to sudden gas leaks that put workers' lives at immediate risk. Because of these factors, the monitoring and management of air quality has become a matter of major global concern. The first and most critical step in addressing this issue is establishing a reliable way to monitor it [10,11,12]. The data obtained, moreover, must be processed and sent to a server using modules such as GSM This research utilizes Field Programmable Gate Arrays (FPGAs) because they offer parallel processing capabilities that provide the real-time performance required for industrial safety.

The system was designed on a Spartan - 3 FPGA using the VHDL language. FPGAs are practical because reprogramability and reusability [13].Hardware Description Languages (HDL) are an excellent design input language. There are two types of HDL which are Verilog and VHDL [14].

Design simulations are performed at the hardware level, for the purpose of verifying the functionality and operation of the system. Compared to micro_controllers, the choosing FPGA provide numbers of I/O ports and the paralle l which implementation the algorithm results in execution device by using GSM interface. The system can be used in isolated areas.

II. Gas_sensor MQ

Gas sensor (MQ-135) is used to measure air_quality and detects the ratio of nitrogen oxides, alcohol, benzene, CO2, Nh3 and smoke. The MQ-135 has a digital output that works with or without a micro_controller. The analog TTL is powered from 5V which used with common micro_controllers [15].

The sensitivity characteristics (MQ-135) for the resistance ratio RS / R0. The resistance RL can be defined as the change in the resistance sensor as a function of gas concentration, and the resistance sensor (RO) is the known concentration in the fresh air [16], Figure (1).

The scale of the graph is log_log on a linear scale. The gas concentration correlates with exponential resistance. The gas concentration data range is

only (10- 200 p.p.m.) and the linear relation seen between gas concentration and resistance coe

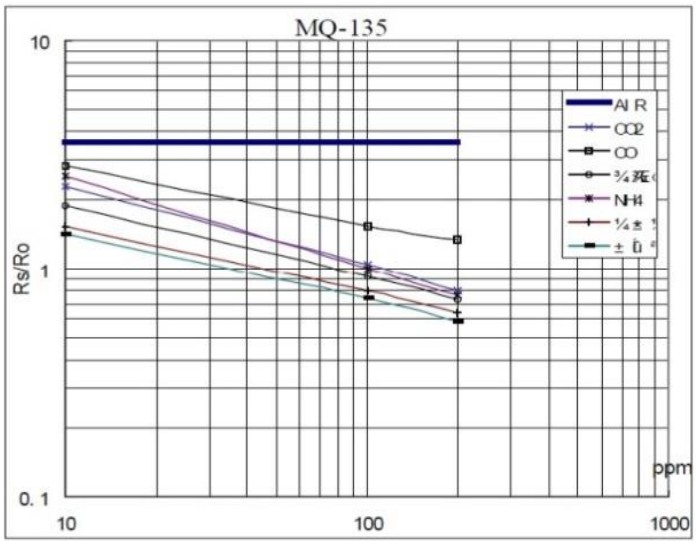


Figure 1. Sensitivity Characteristics_MQ-135

III. FPGA

FPGAs consist of configurable logic blocks (CLBs) that are connected via a two-dimensional array of vertical and horizontal switches, where the intersections of these connections form a Programmable Switch Matrix (PSM). The design's branch circuits were subdivided and assigned to the CLB. Subsequently, the PSMs establish connections between the CLBs. Hardware blocks feature chip ends known as I/O blocks (IOBs), which are used to direct signals into and out of the chip. FPGAs are composed of two fundamental blocks: CLBs and IOBs [18].

CLBs are primarily composed of lookup tables (LUTs), random access memory modules (RAM), and D-flip-flop multiplexers. As illustrated in Figure 2, a LUT can implement any four-input logic gate.

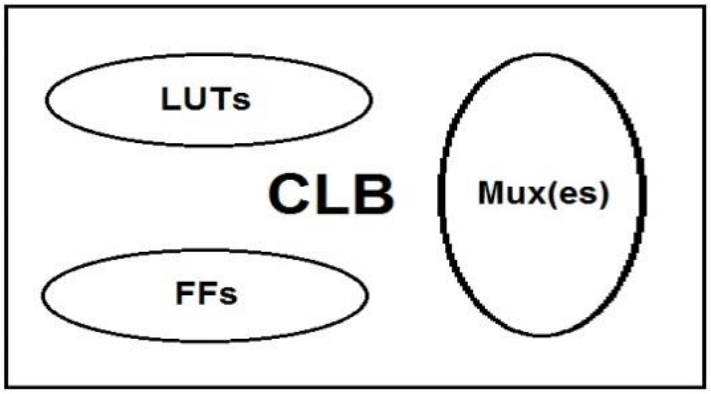


Figure 2. FPGA_Atecture

The blocks can be more complex to be more efficiency and functionality depending on the company making the product.The propagation of the delay of LUTs are independent of functions performed which are a predefined list of output that result from each group of inputs [19] as shown in figure (3).

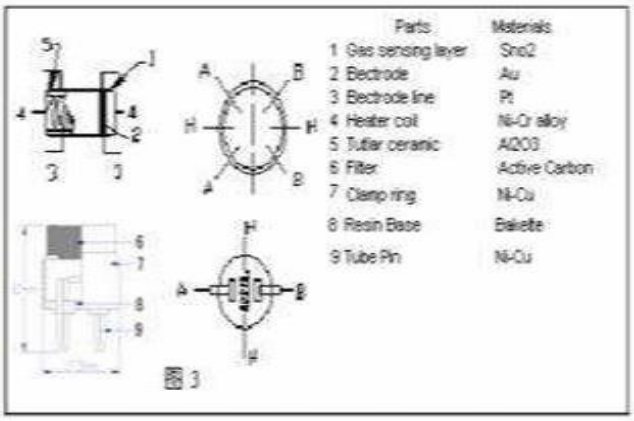


Figure 3. CLB Architecture

The project control chip devices were designed with VHDL and tested with Xilinx. First, we write and simulate VHDL code with Xilinx and implement it on Xilinx Spartan 3 FPGAs to enable easy FPGA connection and programming via the JTAG series. The JTAG interface used to connect the board to PC and create way to send / receive informations [20].The JTAG chain start at the connector , and spans PROM, ACE controller, CPLD and FPGA board series. The main use is to program and access FPGA through

JTAG connection as shown in figure (4).The tool analyses the logic to see the signal or the internal FPGA node of integrated processors and analyses the signals through the JTAG chain through the Chip-Scope Pro Logic Analyser [21].

The objective is to measure the analog signal from pollution sensor. The MQ 35 gas sensor circuit measures the data and transmitted it through the FPGA controller to read and process data. The controller then connects via the serial port to the GSM modem and to the interface circuit [22].The controller unit is mainly composed of the control unit (CU), internal ROM for storage, and a UART (Universal Asynchronous Receiver) for managing data flow. To make the hardware work with external networks, The VHDL code also incorporates connections via AT commands for GSM modems [23,24].

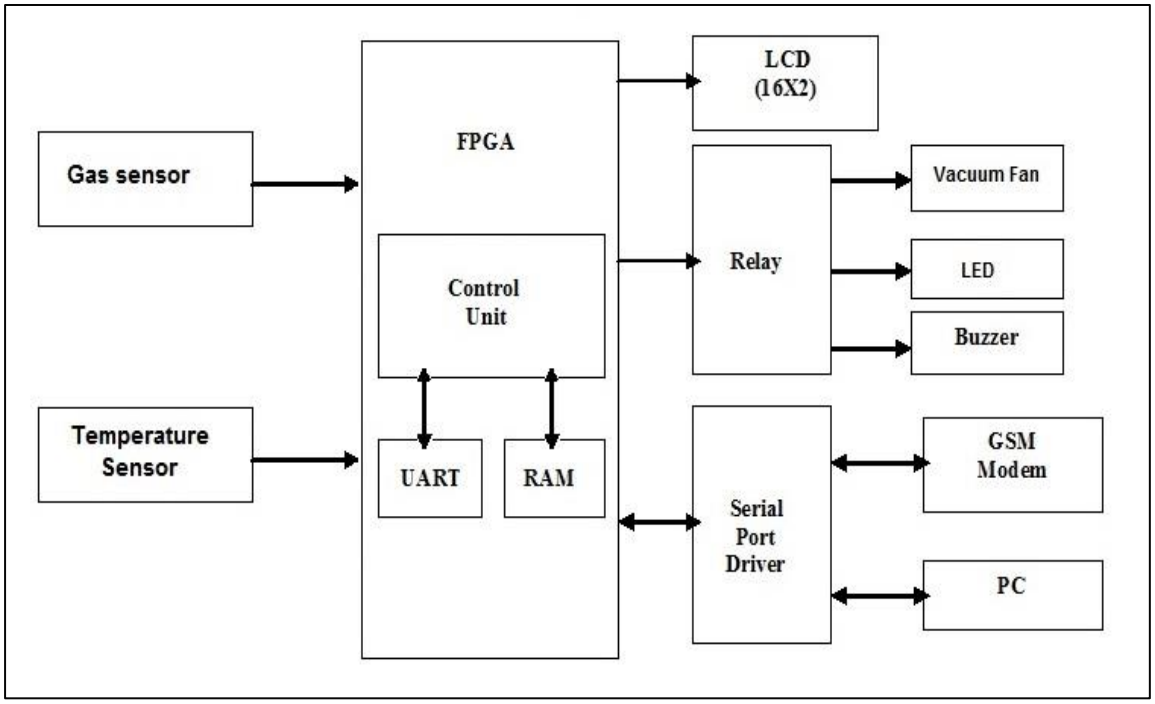


Figure 4. Block Diagram of The System

Where GSM_Rx connected to sensors (inputs) and GSM _Tx connected to devices (output) [25] as shown in figure (5).

4.1 RS232

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
--entity designWithRS232 is
Port ( clk : in STD_LOGIC;
reset : in STD_LOGIC;
send : in STD_LOGIC;
button : in STD_LOGIC;
bitout : out STD_LOGIC);
end designWithRS232;
architecture Behavioral of designWithRS232 is
component counter is
Port ( clk : in STD_LOGIC;
reset : in STD_LOGIC;
send : in STD_LOGIC;
sample : out STD_LOGIC_VECTOR (31 downto 0));
end component;
component rs232 is
Port (samplein STD_LOGIC_VECTOR (31 downto 0);
clk : in STD_LOGIC;
reset : in STD_LOGIC;
send : in STD_LOGIC;
button : in STD_LOGIC;
bitout : out STD_LOGIC);
end component;
signal tempsample : STD_LOGIC_VECTOR (31 downto 0);
begin
p1: counter port map ( clk, reset, send, tempsample );
p2: rs232 port map ( tempsample, clk, reset, send, button, bitout );
end Behavioral;
```

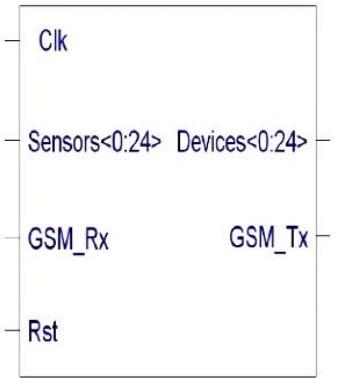


Figure 5. VHDL Up level model

The GSM transmitter and receiver are connected through an RS232 adapter. When receiving data from the GSM module, the voltage level is converted to TTL, whereas when sending data to the GSM modem,(ttl) is converted to RS232 [26].

IV. Implementing

4.2 State Machine

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity sendgetstatemachine is --sends either 0 (get) or 1 (send) everyother clock cycle
Port ( clk : in STD_LOGIC;
send : out STD_LOGIC );
end sendgetstatemachine;
architecture Behavioral of sendgeststatemachine is
signal tempsend : STD_LOGIC := '0'; --levelGsend signal
begin
process (clk) begin
if (clk'event and clk = '1') then --if clk rising, send = not send levelGsend <= not(levelGsend);
else
levelGsend <= levelGsend; --else keep
end if;
send <= levelGsend;
end process;
end Behavioral;
```

V. Convert and Send the Data

The UART receiver (U_0), the memory module (U_1), the sensor unit (U_2), the control unit (U_3) and the UART transmitter (U_4) are the most important components of VHDL. The primary function of a UART receiver

is to receive serial data from a GSM modem and convert it into parallel data for processing. [27].

The control unit system creates AT commands, processes received SMS_messages and content messages. Also in an emergency situation sending system commands and SMS_messages to concerned case management. The UART transmitter have main function which is convert the processed data from parallel to serial , then send the data s serially to the GSM modem [28].

VI. Results

System tested via PCS serial port and real time via GSM. The simulation of a controller is sending data in parallel to (UART) transmitter. AT commands sends to read the message at position 1 "AT + CMGD = 1" and uses the characters "$" to start transmitted data ,and "#" to end the transmitted data as shown in Figure (6). UART transmitted data in two states: the first is displaying data in a 10-bit frame and the next case is to sending a frame to the output sequential (S_out), Where (k) represents the counter for the number of bits to be transmitted in the second state, for which both Tx_req and Tx_ are ready for a handshake as shown in Figure (7). The UART received data , where reg_GSM represents the offset register, the S_in serial data input becomes reg_GSM after the start bit is received, and when rx_en is high, after the 8-bit Receiver offset character and stop bit, ASC Ⅱ character must be mapped to reg_GSM on P_out as shown in Figure (8).

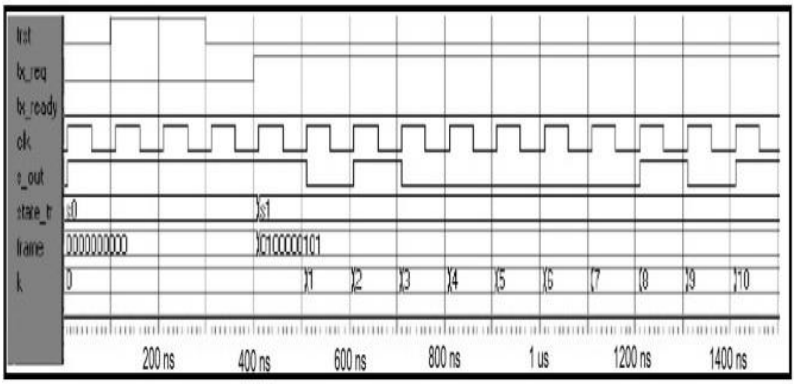


Figure 6.Control Unit sending AT command

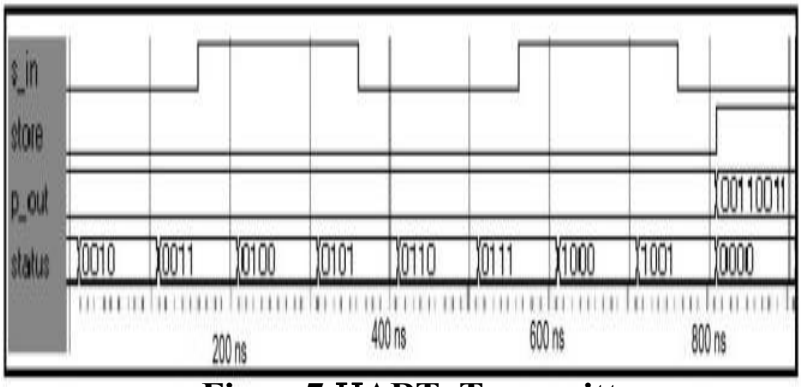


Figure7.UART_Transmitter

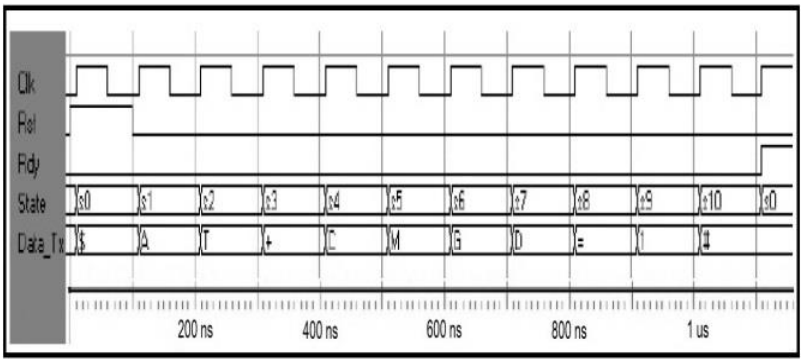


Figure 8.UART_ Receiver

VII. The strengths and effectiveness of the design

The proposed design are shown to be effective in terms of the specific architectural benefits that can be provided:

Reprogrammability and Reusability: FPGAs are also practical because they can be reprogrammed and reused to make updates and modifications without changing the hardware.

Compact and Scalable: The system is compact and can be scaled up or down to suit various spaces, both indoor and outdoor. In addition, the system can be easily scaled up for larger industrial applications.

Industrial Safety in Isolated Areas: The integration with a GSM modem enables the system to send real-time SMS alerts to the operators if the pollution level is above a permissible limit. This makes it very effective in isolated and hazardous areas where humans can't be there at all times.

Efficient Data Handling: It uses a UART (Universal Asynchronous receiver) and a control unit for data flow and for generating AT commands to be fed to the GSM modem to ensure reliable data communication between the sensors and operator.

VIII. CONCLUSION

A controller design present automating pollution detection sensors appended with FPGA and GSM. The system is implemented on a Spartan-3 FPGA hardware platform, utilizing a specialized design language called VHDL. All equipment and for the entire system designed are simulated and tested. FPGA was chosen because it provides more I / O_ ports, and hardware parallel implementation results with faster execution of algorithms. The GSM interact with the FPGA through the GSM interface. The result is an inexpensive system and can be easily scaled up. The system can be used in an isolated and dangerous range. It should be borne in mind that the S1M card placed in the unit must be activated to use GPRS periodically. The readings obtained from the sensors are not quite equal to the values obtained using high-end devices, but they are still much closer. The proposed model can be well used indoors as well as outdoors due to its compact structure and efficiency. The paper achieves its goal of a lower cost product with higher efficiency in this model.

IX. ACKNOWLEDGEMENTS

Thanks to the Department of Computer Science at Mustansiriyah University-IRAQ for their assistance with this research, which authors gratefully acknowledge.

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نظام ذكي لمراقبة والتحكم في تلوث الغاز عبر مصفوفة البوابات القابلة للبرمجة ميدانيًا و النظام العالمي للاتصالات المتنقلة

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ملاحظة : هل البحث مستل من رسالة ماجستير او اطروحة دكتوراه ؟ نعم : كلا : √

المستخلص:
تمتلك مصفوفات البوابات القابلة للبرمجة ميدانيًا (FPGA) قدرة على المعالجة المتوازية، وتوفر هذه المعالجة السريعة متطلبات زمنية وأدائية فورية للتطبيقات الصناعية. الهدف من المشروع هو استخدام حساس متصل بوحدة التحكمFPGA ، التي تقرأ البيانات وتعالجها. ترتبط دائرة الواجهة في وحدة التحكم FPGA بمودم GSM. إذا تجاوزت قيم التلوث المستويات المسموح بها، سيتم إرسال تنبيه إلى المشغل والأشخاص المعنيين الآخرين عبر رسالة نصية قصيرة (SMS) عبر GSM. يهدف المشروع إلى تصميم تطبيق صناعي باستخدام FPGA لقياس تلوث الغاز بهدف تحقيق تكامل أعلى للنظام وتقليل التكلفة في التطوير.

الكلمات المفتاحية: مصفوفة البوابات القابلة للبرمجة ميدانيًا ، النظام العالمي للاتصالات المتنقلة ، لغة وصف العتاد ، لغة وصف العتاد ، حساس غاز ، كتل المنطق القابلة للتكوين، كتل الإدخال والإخراج، جداول البحث ، واجهة اختبار وبرمجة